**CLAIM AMENDMENTS:**

Claim 1 (canceled).

Claim 2 (previously presented): The combined semiconductor apparatus according to claim 5, wherein said planarized region is a part of said surface of said semiconductor substrate which has been subjected to a planarizing process.

Claim 3 (previously presented): The combined semiconductor apparatus according to claim 5, wherein said planarized region is disposed above said integrated circuit of said semiconductor substrate.

Claim 4 (previously presented): The combined semiconductor apparatus according to claim 5, wherein said planarized region is disposed in a region of said semiconductor substrate adjacent to said integrated circuit of said semiconductor substrate.

Claim 5 (currently amended): A combined semiconductor apparatus, comprising:

a semiconductor substrate having an integrated circuit formed therein;

~~a planarized region formed in a surface of said semiconductor substrate;~~

a semiconductor thin film including at least one semiconductor device and bonded on ~~said~~ a planarized region defined on a surface of said semiconductor substrate; and

a planarized film disposed between said planarized region and said semiconductor thin film, wherein a surface of said planarized film on a side of said semiconductor thin film has been subjected to a planarizing process.

Claim 6 (Original): The combined semiconductor apparatus according to claim 5, wherein said planarized film includes:

an electrically conductive layer; and

an interdielectric layer formed in a region peripheral to said electrically conductive layer.

Claims 7 and 8 (Canceled).

Claim 9 (previously presented): The combined semiconductor apparatus according to claim 5, wherein said semiconductor thin film has a common electrode layer on a second surface of the semiconductor thin film opposed to a first surface of the semiconductor thin film, in which said semiconductor device is formed, and

said second surface of said semiconductor thin film is disposed on a side of said planarized region of said semiconductor substrate.

Claim 10 (Original): The combined semiconductor apparatus according to claim 9, wherein said integrated circuit includes individual electrode terminals;

said apparatus further comprising individual interconnecting lines formed on a region extending from an upper surface of said semiconductor device to said individual electrode terminal.

Claims 11- 15 (Canceled).

Claim 16 (previously presented): The combined semiconductor apparatus according to claim 5, wherein said semiconductor thin film is made of compound semiconductor as a main materials.

Claim 17 (previously presented): The combined semiconductor apparatus according to claim 5, wherein said at least one semiconductor device is any of a light-emitting element, a light-sensing element, a Hall element and a piezoelectric element, and said integrated circuit includes a driving-IC for driving said at least one semiconductor device.

Claim 18 (previously presented): The combined semiconductor apparatus according to claim 5, wherein said at least one semiconductor device is a plurality of said semiconductor devices arranged in said semiconductor thin film.

Claim 19 (previously presented): The combined semiconductor apparatus according to claim 5, wherein said at least one semiconductor device is a single semiconductor device disposed in said semiconductor thin film.

Claim 20 (previously presented): An optical print head including the combined semiconductor apparatus of claim 5.

Claims 21-25 (Canceled).

Claim 26 (currently amended): A combined semiconductor apparatus, comprising:

a semiconductor substrate having an integrated circuit;

~~a planarized region formed in a surface of said semiconductor substrate;~~

a semiconductor thin film including at least one semiconductor device and bonded on ~~said~~ a planarized region defined on a surface of said semiconductor substrate;

an integrated circuit device disposed on said semiconductor substrate;

a raised layer formed on a surface of said semiconductor substrate in a region adjacent to said integrated circuit device, an upper surface of said raised layer being at a position higher than an upper surface of said integrated circuit device; and

another semiconductor thin film bonded on the upper surface of said raised layer.

Claim 27 (Previously Presented): An optical print head including the combined semiconductor apparatus of claim 26.

Claim 28 (Previously Presented): An image-forming apparatus comprising at least one optical print head including the combined semiconductor apparatus of claim 26.

Claim 29 (previously presented): The combined semiconductor apparatus according to claim 5, wherein a first surface of said semiconductor thin film, in which said semiconductor device is formed, is disposed on a side of said semiconductor substrate.

Claim 30 (previously presented): The combined semiconductor apparatus according to claim 26, further comprising an electrically conductive layer disposed between said semiconductor substrate and said semiconductor thin film.

Claim 31 (previously presented): The combined semiconductor apparatus according to claim 30, further comprising an interdielectric layer

disposed between said semiconductor substrate and said semiconductor thin film and in a region peripheral to said electrically conductive layer.

Claim 32 (previously presented): The combined semiconductor apparatus according to claim 26, wherein said semiconductor thin film includes a common electrode layer on a second surface of said semiconductor thin film opposed to said first surface, and said integrated circuit has a common electrode terminal;

said apparatus further comprising a common interconnecting layer formed on a region extending from an upper surface of said common electrode layer of said semiconductor thin film to said common electrode terminal of said integrated circuit.

Claims 33 and 34 (canceled).

Claim 35 (new): The combined semiconductor apparatus according to claim 5, wherein said planarized region has a flatness not greater than 10 nanometers.

Claim 36 (new): The combined semiconductor apparatus according to claim 26, wherein said planarized region has a flatness not greater than 10 nanometers.